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Serial No.
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LIST OF PATENTS AND PUBLICATIONS
FOR APPLICANT'S INFORMATION
DISCLOSURE STATEMENT
(Use Several Sheets if Necessary)

Applicant
Howard G. Sachs

Filing Date
November 5, 1993

Group
Unknown

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Subcl:	File Date If Approp
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VAD AA 4,847,755 7/11/89 Morrison, et al. 364/200

AB

FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Class	Subcl:	Trans. Yes No
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AD

AE

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

VAD AG ✓ Bakoglu, H. B., et al., "The IBM RISC System/6000 Processor: Hardware Overview," IBM J. Res. Develop. (January 1990) 34(1):12-22.

VAD AH ✓ Fisher, Joseph A., et al., "Parallel Processing: A Smart Compiler and a Dumb Machine," Proceedings of the ACM SIGPLAN '84 Symposium on Compiler Construction, SIGPLAN Notices (June 1984) 19(6):37-47.

VAD AI ✓ Agerwala, Tilak, et al., "High Performance Reduced Instruction Set Processors," IBM Research Report No. 12434 (#55845) (1/9/87), IBM Thomas J. Watson Research Center, Yorktown Heights, New York.

VAD AJ ✓ Patterson, David A., et al., Computer Architecture -- A Quantitative Approach, Morgan Kaufmann Publishers, Inc., San Mateo, Calif., 1990, Table of Contents, pp. xi-xv.

EXAMINER

DATE CONSIDERED

Valerie Darch

4-14-94

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.